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| Subclass | Class | ISSUE CLASSIFICATION |
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PATENT NUMBER

U.S. UTILITY Patent Application

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| O.I.P.E. | | PATENT DATE |
| SCANNED 115 | Q.A. CH | |

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| APPLICATION NO. | CONT/PRIOR | CLASS | SUBCLASS | ART UNIT | EXAMINER |
| 09/558377 | F | 709 | 711 | 2758 | VERBRUGGE Ramanathan |

APPLICANTS
Jean-Francois Autechau

TITLE
Modular interconnection architecture for an expandable multiprocessor machine, using a multilevel bus hierarchy and the same building block for all the levels

PTO-2040
12/99

| ISSUING CLASSIFICATION | | | | | |
|--|----------|--------------------|-----------------------------------|--|--|
| ORIGINAL | | CROSS REFERENCE(S) | | | |
| CLASS | SUBCLASS | CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | |
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| INTERNATIONAL CLASSIFICATION | | | | | |
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| □ Continued on Issue Slip Inside File Jacket | | | | | |

| □ TERMINAL DISCLAIMER | DRAWINGS | | | CLAIMS ALLOWED | |
|--|---|-------------|------------|----------------------------|----------------------|
| | Sheets Drwg. | Figs. Drwg. | Print Fig. | Total Claims | Print Claim for O.G. |
| □ The term of this patent subsequent to _____ (date) has been disclaimed. | (Assistant Examiner) _____ (Date) | | | NOTICE OF ALLOWANCE MAILED | |
| □ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ | | | | ISSUE FEE | |
| □ The terminal _____ months of this patent have been disclaimed. | (Primary Examiner) _____ (Date) | | | Amount Due | Date Paid |
| | | | | ISSUE BATCH NUMBER | |
| | (Legal Instruments Examiner) _____ (Date) | | | | |

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